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EMC and Signal Integrity

IMEC Course Advanced Packaging

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Agenda

- **Signal and Power Integrity on PCB**
  - Introduction
  - Impedance controlled lines
  - Crosstalk
  - Parasitics
  - Power integrity issues
  - Decoupling
- **EMC/EMI on PCBs**
- **PCB design guidelines**

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What is Signal and Power Integrity?

- **Signal Integrity ensures signals are of sufficient quality to reliably transmit their required information, and do not cause problems to themselves or to other components in the system.**
- **Signal Integrity applies to Digital, Analog and Power electronics**
- **Signal Integrity issues are more common now because electronics are more dense and chips have faster rise times**
  - Assuring Signal Integrity now involves more knowledge of such RF techniques as terminations, impedance matching
- **Major function of engineering, next to conceiving the correct design, is implementing the design correctly**
- **Signal integrity assures the circuit design operates as intended and must be designed in.**
  - Correct design relies on experience, best practices, analysis and simulation to ensure desired signal quality.

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Designing the system correctly

- **Fundamentally, signal integrity must be designed in and not "discovered" by test.**
  - Tests verify that signals have the intended integrity.
  - Tests are not designed to qualify a poor design
- **Each designer identifies the critical signals and ensures their integrity is not compromised.**
- **Critical signals are supported by analysis, modeling, or technical rationale justifying why they are expected to work.**
- **Identified critical signals receive special layout attention assuring their proper functioning**
- **Signal Integrity analysis, test results, and scope pictures should be available at the final design review**

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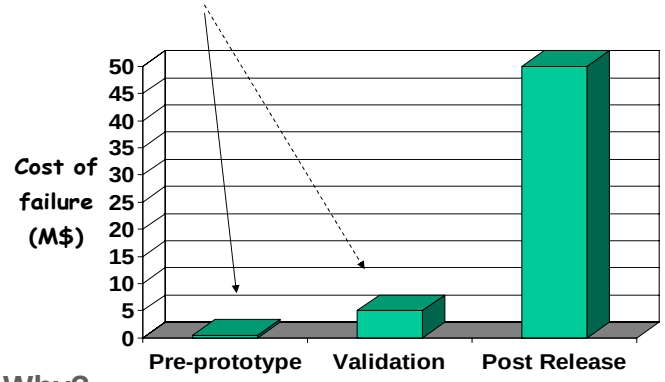
Effective SI is Pre-Product Release

- **It costs less here**



- **Why?**
  - Time = $

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When are frequencies high?

Rule of thumb:

$$\text{line length } \ell > \text{wavelength at highest frequency} / 10$$

What does this mean for data communication?

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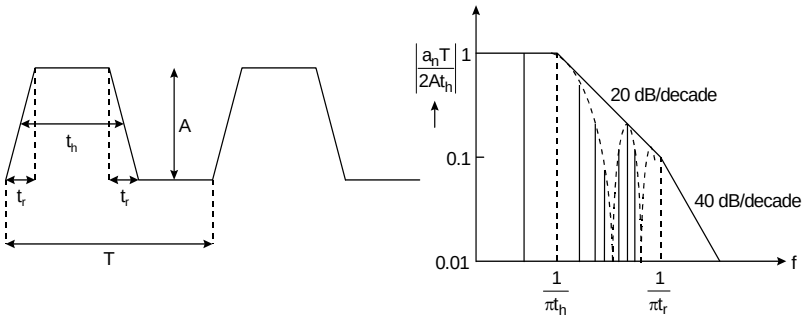
Data signal bandwidth



- fourier transform (periodic signal): discrete components at frequencies $f_n = nf_T = \frac{n}{T}$
- highest frequency: approximation to $\frac{1}{\pi t_r}$

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Data signals: high-frequency effects

- rule of thumb: line length ℓ > wavelength at highest frequency / 10
- highest frequency: $\frac{1}{\pi t_r} \Rightarrow \lambda_{min} = \frac{v_{ph}}{f_{max}} = v_{ph}\,\pi t_r$
- delay of signal: $\tau = \frac{\ell}{v_{ph}}$ (no dispersion assumed)

$$\Rightarrow \quad \ell > \frac{\lambda_{min}}{10} \text{ or } \tau\, v_{ph} > \frac{v_{ph}\,\pi t_r}{10}$$

$$\text{or} \quad 3.2\tau > t_r$$

$$\text{in literature} \quad \boxed{3.5\tau > t_r}$$

EXAMPLE:

$t_r = 2$ ns, $f_{max} = 160$ MHz
microstrip $(\varepsilon_r = 4) \Rightarrow v_{ph} = 17.7$ cm/ns

$$\lambda_{min} = \frac{17.7\,10^7}{160\,10^8} = 111\,\text{cm} \Rightarrow \ell > 11\,\text{cm}$$

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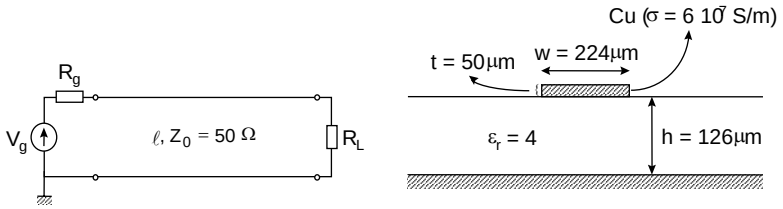
Data signals: high-frequency effects



Case 1: ℓ = 5 cm and τ = 0.28 ns; R_L = 1000 Ω

Case 2: ℓ = 20 cm and τ = 113 ns; R_L = 1000 Ω

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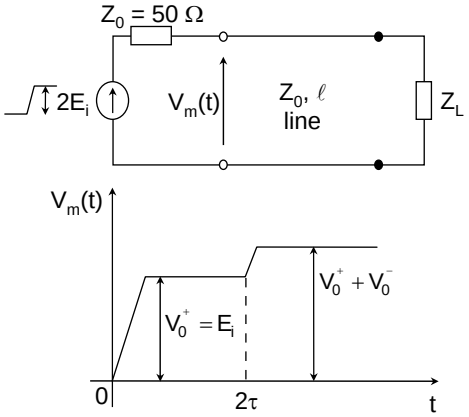
Time-domain propagation and reflection



$V_0^+ = E_i$

Γ = reflection coefficient corresponding to Z_L with respect to Z_0

$$= \frac{V_0^-}{V_0^+}$$

$$= \frac{Z_L - Z_0}{Z_L + Z_0}$$

$\Rightarrow$ measurement of $V_0^- \Rightarrow$ determination of Z_L
(basis of Time Domain Reflectometry)

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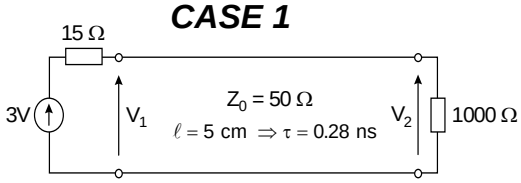
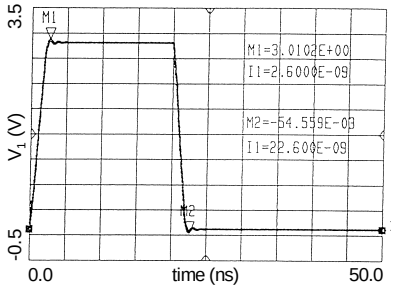
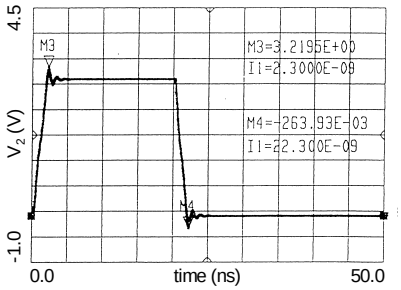
Data signals: high-frequency effects

CASE 1







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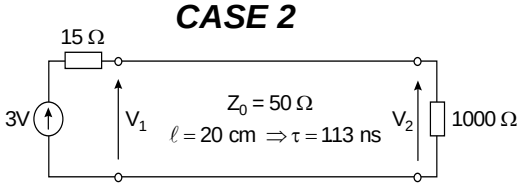
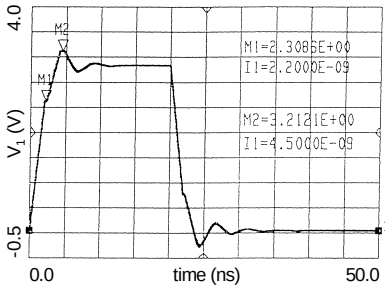
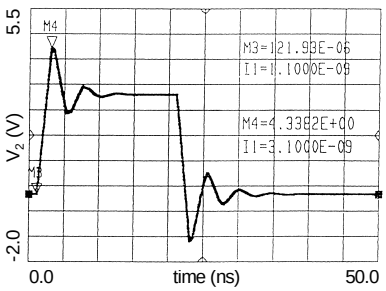
Data signals: high-frequency effects

CASE 2







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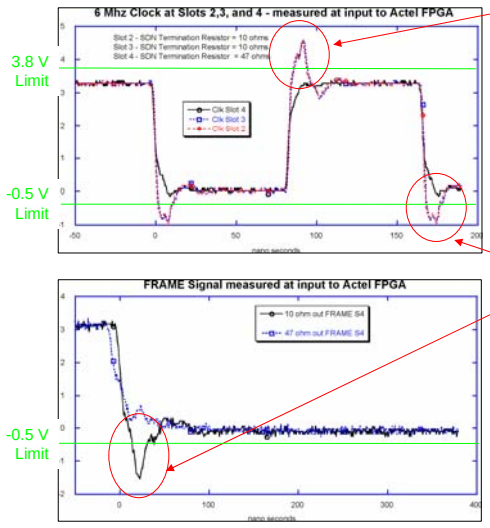
Practical example



- **Significant and Unacceptable Over- and Undershoot**

From: Ed James, GSFC, ACE Signal Integrity Tuning

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Impact of over/undershoot and ringing

- **Undershoot / Overshoot**
  - The undershoot/overshoot may cause damage to the ICs by damaging input protection circuitry.
  - In some situations reflections are required for circuit operation – i.e.., PCI bus signals, which use reflected wave signaling.
- **Ringing**
  - Ringing can distort the appearance of signals, causing signal transitions to be smaller or larger at the receiver.
  - Can also cause damage to ICs.
  - Ringback problems can also cause incorrect logic switching if the voltage falls between the threshold voltage range.

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Summary high-frequency effects of lines

Short rise times as high frequencies (t_r < 3.5 x delay of line)

↓

PCB tracks = transmission lines

↓

Reflections at mismacthes

↓

Over/undershoot and ringing on signals

↓

solution?

↙ ↘

Proper termination

Linelength long enough such that ringing has no effect

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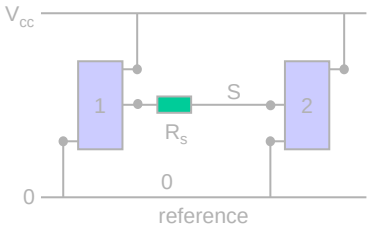
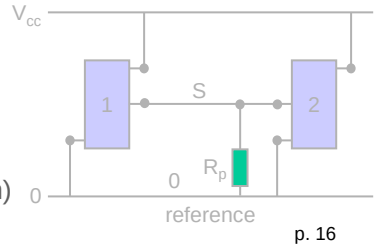
Serial and DC parallel matching

- **Serial termination**
  - *Advantage:* small space on board or even intergrated in chip
  - *Drawback:* voltage over R_s may become large
- **Parallel termination**
  - *Advantage:* No loading of signal
  - *Drawback:* power dissipation in resistor
  - Note: active termination such as diodes could limit over- and undershoots (less power consumption)





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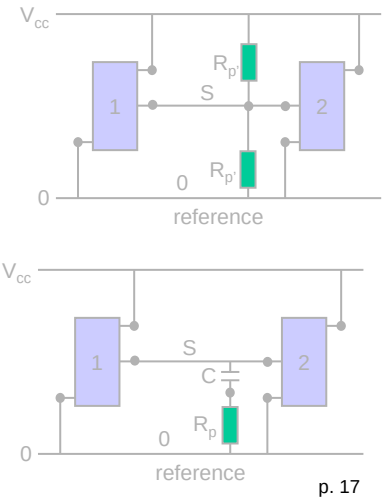
Thevenin and AC parallel matching

- **Thevenin termination**
  - Similar to parallel, but with two resistors one to Vcc and one to Gnd or reference.
  - Provides pullup-pulldown function as well as termination.
- **AC termination**
  - *Advantage:* Capacitor blocks DC current, so no steady state current as with DC parallel.
  - *Drawback:* capacitor might effect the rise/fall times of the signal



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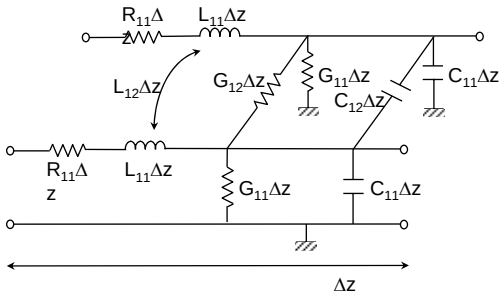
Coupled lines

$$\overline{\overline{R}} = \begin{bmatrix} R_{11} & 0 \\ 0 & R_{11} \end{bmatrix} \qquad \overline{\overline{G}} = \begin{bmatrix} G_{11}+G_{12} & -G_{12} \\ -G_{12} & G_{11}+G_{12} \end{bmatrix}$$

$$\overline{\overline{L}} = \begin{bmatrix} L_{11} & L_{12} \\ L_{12} & L_{11} \end{bmatrix} \qquad \overline{\overline{C}} = \begin{bmatrix} C_{11}+C_{12} & -C_{12} \\ -C_{12} & C_{11}+C_{12} \end{bmatrix}$$



R = resistance matrix
G = conductance matrix
L = inductance matrix
C = capacitance matrix

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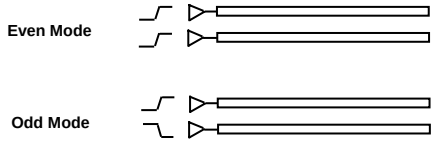
Odd and Even transmission modes

- Electromagnetic fields between two driven coupled lines will interact with each other
- These interactions will effect the impedance and delay of the transmission line
- A 2-conductor system will have 2 propagation modes
  - Even Mode (Both lines driven in phase)
  - Odd Mode (Lines driven 180° out of phase)



- The interaction of the fields will cause the system electrical characteristics to be directly dependent on patterns

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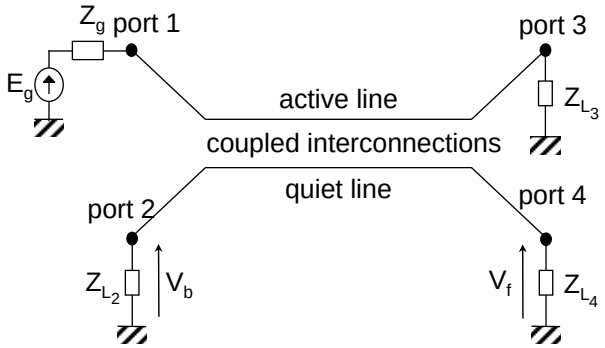
Crosstalk



V_b = backward crosstalk [V]
V_f = forward crosstalk [V]

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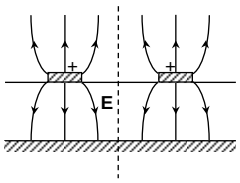
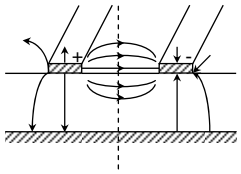
Symmetrically coupled lines

Even or common mode



symmetry plane

Odd or differential mode



symmetry plane

$$Z_e = \sqrt{\frac{L_{11}+L_{12}}{C_{11}}} \geq Z_o = \sqrt{\frac{L_{11}-L_{12}}{C_{11}+2C_{12}}}$$

$$v_e = \frac{1}{\sqrt{(L_{11}+L_{12})C_{11}}} \leq v_o = \frac{1}{\sqrt{(L_{11}-L_{12})(C_{11}+2C_{12})}}$$

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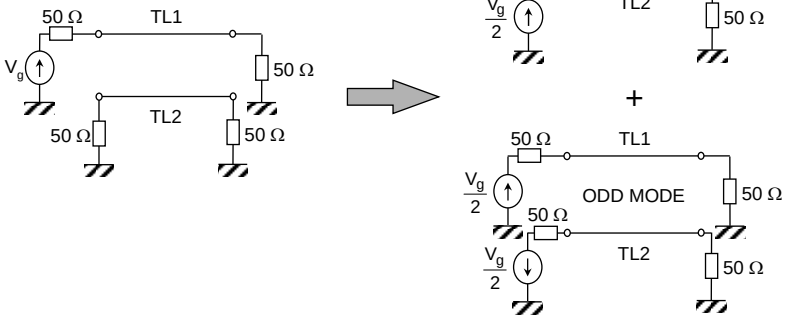
Relation crosstalk and even/odd mode



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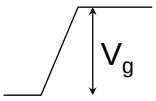
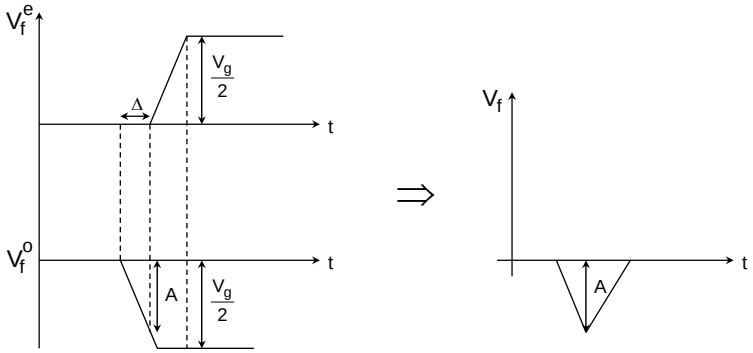
Forward crosstalk

$v_e < v_o \Rightarrow \tau_e > \tau_0$

$\Delta = \tau_e - \tau_0$





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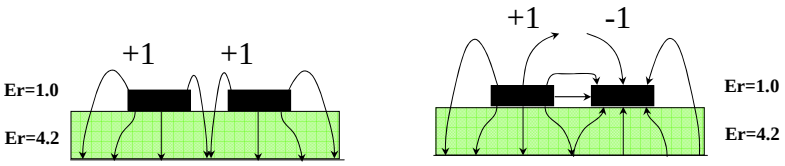
Microstrip vs. Stripline Crosstalk

- Odd and Even mode electric fields in a microstrip will have different percentages of the total field fringing through the air which will change the effective Er (permittivity)
  - Leads to velocity variations between even and odd mode

Microstrip E field patterns



- The effective dielectric constant, and subsequently the propagation velocity depends on the electric field patterns

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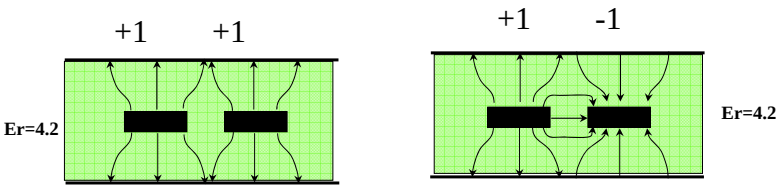
Microstrip vs. Stripline Crosstalk

- If the dielectric is homogeneous (I.e., buried microstrip or stripline) , the effective dielectric constant will not change because the electric fields will never fringe through air

Stripline E field patterns



- Consequently, the velocity must stay constant between even and odd mode patterns
- The constant velocity in a homogeneous media (such as a stripline) forces far-end crosstalk noise to be zero

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Impact of crosstalk

- Crosstalk can add up if traces run parallel of each other over longer lengths on the PCB
- Crosstalk can also be induced if the trace spacing is reduced
- High density PCBs yield more crosstalk
- Crosstalk can be mitigated by laying out circuit traces appropriately – taking consideration of vertical/horizontal routing, trace width and spacing.
- Differential and even mode termination helps reducing crosstalk

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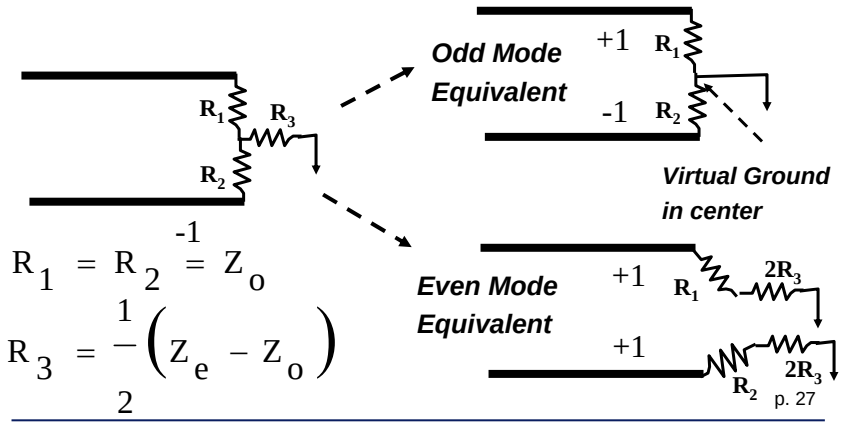
Odd- and even-mode termination

- 3 resistor networks can be designed to terminate both odd and even modes
- T-termination



$$R_1 = R_2 = Z_o$$

$$R_3 = \frac{1}{2}\left(Z_e - Z_o\right)$$

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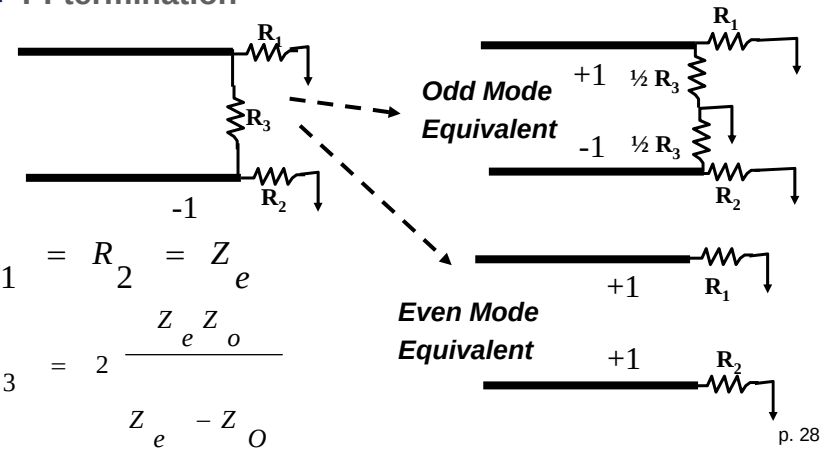
Termination

- The alternative is a PI-termination
- PI-termination



$$R_1 = R_2 = Z_e$$

$$R_3 = 2\,\frac{Z_e Z_o}{Z_e - Z_O}$$

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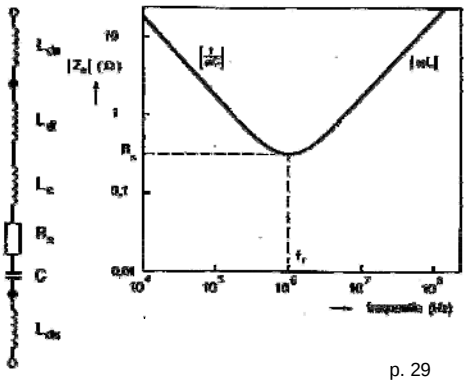
Parasitics of passive components

- Don't forget to take into account parasitics of R, L and C
- E.g. capacitor is above resonance frequency inductive!
- Circuit model
  - L_{du} = inductance of external wire
  - L_{di} = inductance of internal wire
  - L_C = inductance due to construction of capacitor
  - R_S = resistance representing losses



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Parasitics of passive components

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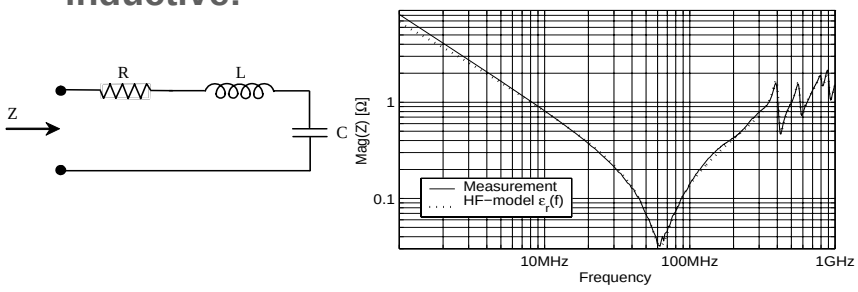
- Capacitor is above resonance frequency inductive!



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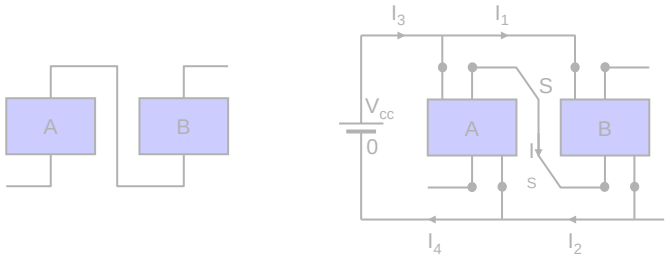
The power supply circuit

- **Add power circuit to functional diagram**



- Return currents in ground and power supply circuit
- Transmission line is not defined
- Power supply tracks are also transmission lines!
- Large loops may exist!

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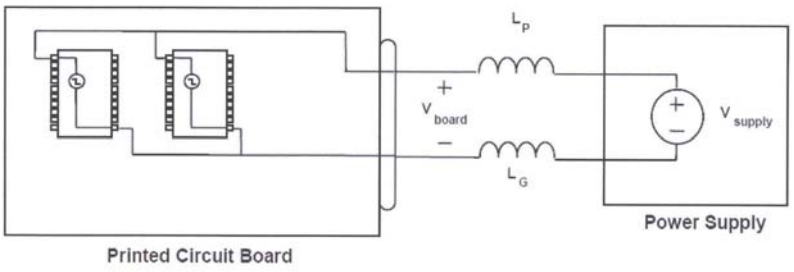
Circuit model up to 5 MHz



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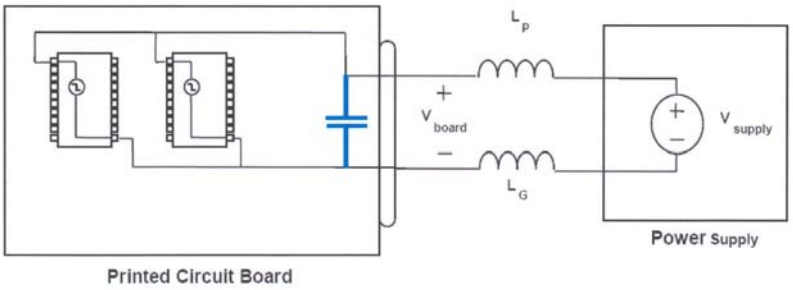
Adding Elco capacitor

- **Influence of long power supply lines**

  ⇒ Use of elco capacitor (functions as local power supply)



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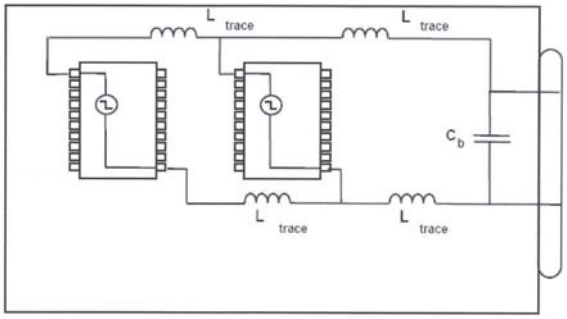
Circuit model 5-50 MHz

- **PCB without power and ground planes**



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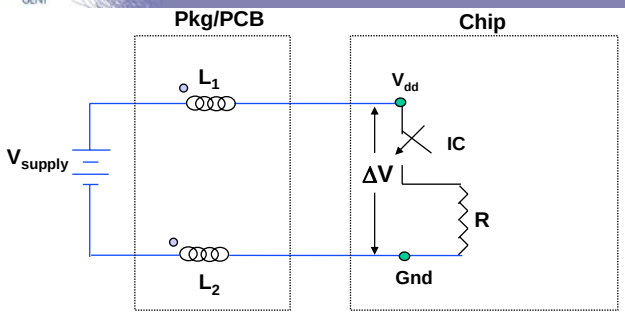
Power Supply Noise



- Inductance in the power supply loop causes power supply noise
- Causes fluctuations on the chip supply tracks

$$\Delta V = L_{eff} \, (dI/dt)$$

Current Transition

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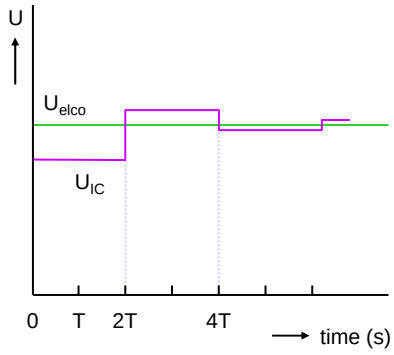
Voltage variation

- Voltages at Elco and input IC
- Voltage variations reduce noise margin



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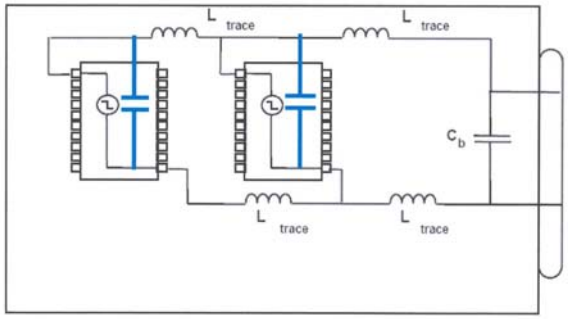
Adding decoupling capacitors

- **PCB without ground and power planes**



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Design decoupling capacitor

- **Assumptions**
  - maximum allowed voltage variation = 0.1 V
  - technology assumptions: current drawn in or out power supply circuit = 35 mA and duration of current pulse = 10 ns

$$\Delta I = C_d \frac{\Delta U}{\Delta t} \approx C_d \frac{\Delta U}{t_s}$$

ΔI = 35 mA, t_s = 10 ns, ΔU = 0.1 V
$\Rightarrow C_d$ = 3.5 nF

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Influences decoupling capacitors

- **Influence of inductances**
  - Package pin and bond wire: e.g. L ≈ 20 nH
  - ΔU_L because of ΔI

$$\Delta U_L = L\frac{\Delta I}{\Delta t} \approx L\frac{\Delta I}{t_s},\ \Delta I = 35\,mA, t_s = 10\,ns, L = 20\,nH \Rightarrow \Delta U_L = 0.07\,V$$

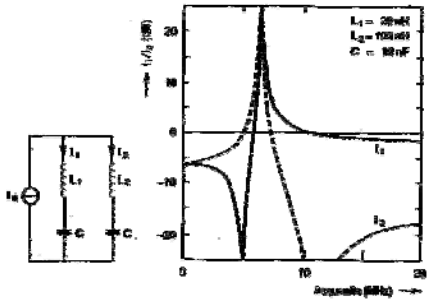
⇒ **Noise margin is reduced**

- **Capacitors in parallel**
  - Resonance frequencies

$$\omega_1 = \sqrt{\frac{2}{(L_1 + L_2)C}}$$

$$\omega_2 = \frac{1}{\sqrt{L_2 C}}$$

$$\omega_3 = \frac{1}{\sqrt{L_1 C}}$$



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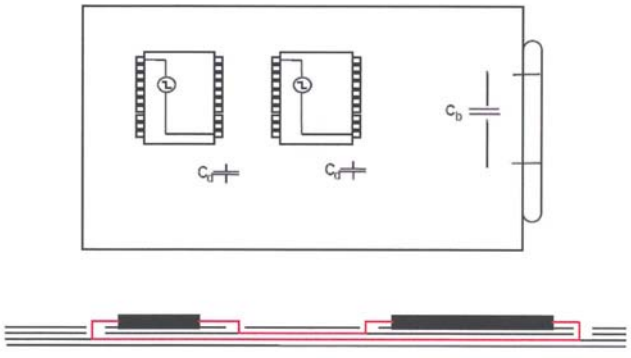
Circuit model 50 – 500 MHz

- **PCB with power and ground planes**



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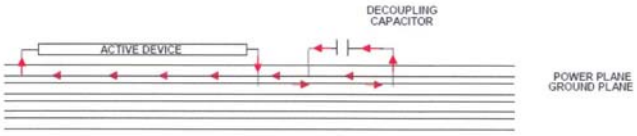
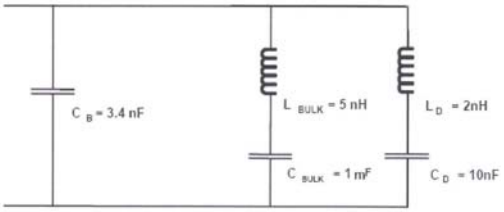
Modelling PCBs with planes





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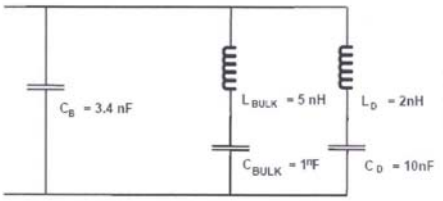
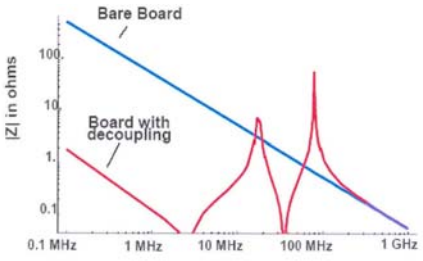
Modelling PCBs with planes





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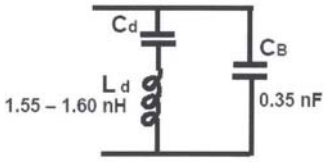
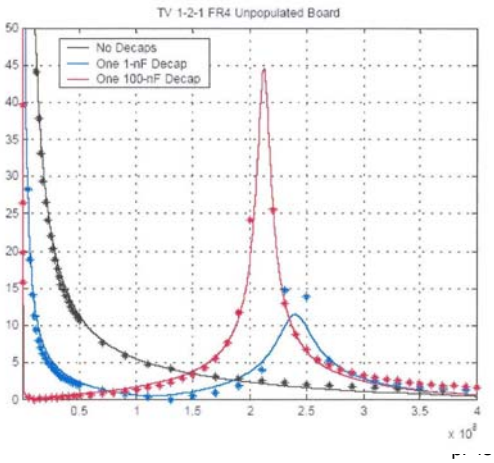
Modelling PCBs with planes





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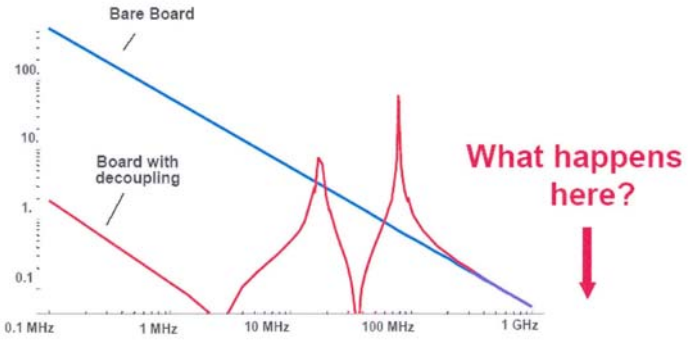
Model of planes above 500 MHz



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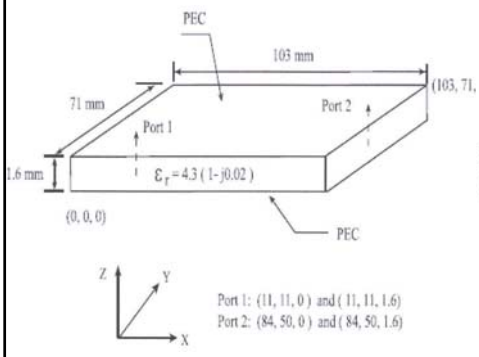
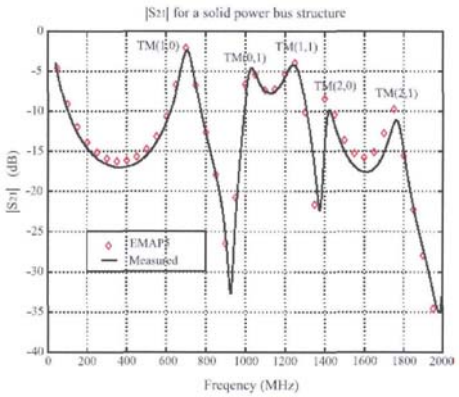
Power bus resonance





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Agenda

- **Signal and Power Integrity on PCB**
  - Introduction
  - Impedance controlled lines
  - Crosstalk
  - Power integrity issues
  - Decoupling
- **EMI/EMC on PCBs**
- **PCB design guidelines**

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What Is EMI / EMC?

- EMI - Electromagnetic Interference is any electric or magnetic emission from a device or system that interferes with the normal operation of another device or system.
- EMC - Electromagnetic Compatibility is the ability of a device or system to function without error (susceptibility) in its intended electromagnetic environment.

EMI / EMC is not Black Magic!

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Higher bitrates and EMC

Trend: higher bitrates in digital systems

Higher bandwidths

Intra-system EMC
- Increased crosstalk
- Disturbance signals, inductance wirebonds, ...

Inter-system EMC
- Enhanced radiation

Rule of thumb: always use lowest required bit rate

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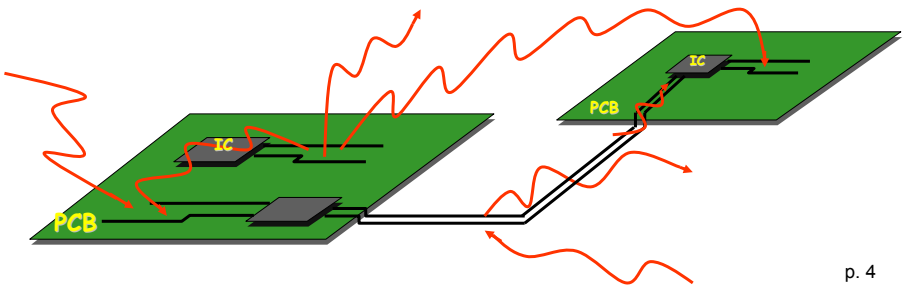
PCB interference (EMI)

- **Electronic circuits produce and are subject to Electromagnetic Interference (EMI).**
  - in particular when wavelengths ~ wire lengths
- **EMI is a problem because it can severely and randomly affect analog and digital circuit functionality!!!**



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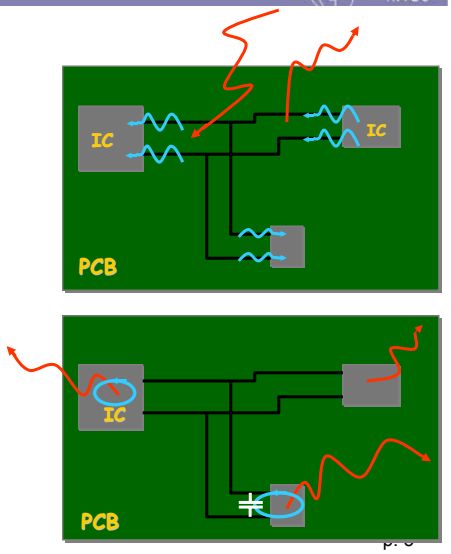
EMI at board, package and IC level

- Traces on PCB can pick up **EMI** and transmit it to IC's
- IC's can produce high frequency **conducted emissions** that can **radiate** from PCB's
- IC's themselves can directly produce **radiated emissions**
  - high-frequency current loops Vdd-decap-gnd on package or inside IC's.
  - high-frequency current loops inside IC (near future)
  - IC radiation amplified by heat sinks!



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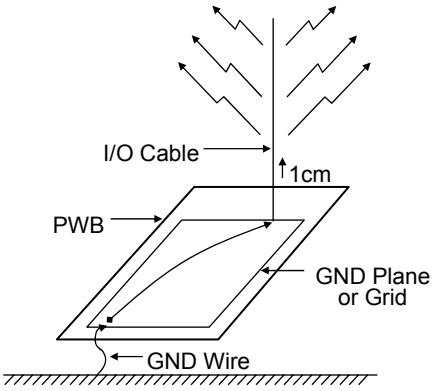
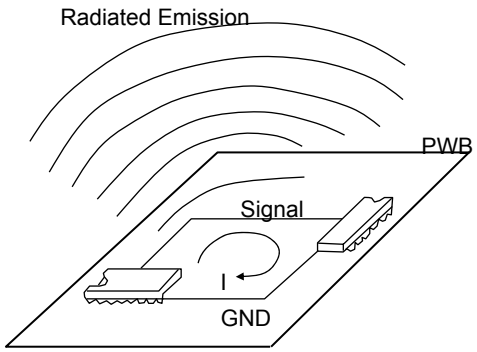
Common & Differential Mode radiation



Common mode radiation
(monopole type)



Differential mode radiation
(loop type)

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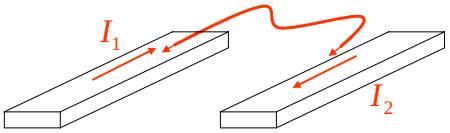
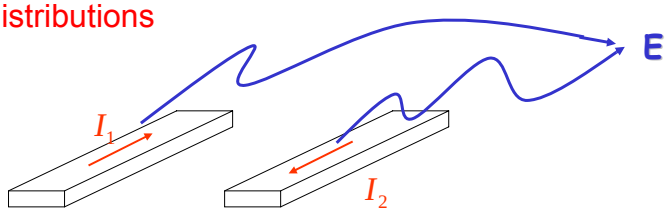
EMI analysis: solution procedure

- **Typically, EMI analysis is a two-step process:**
  - 1) determine accurately current distributions on conductors



  - 2) calculate radiated fields from the current distributions



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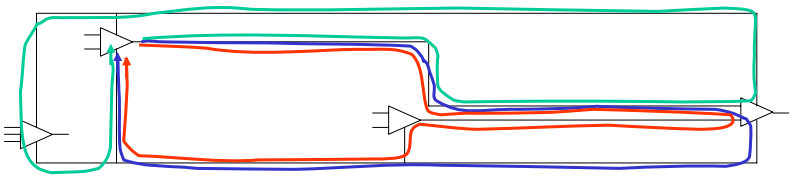
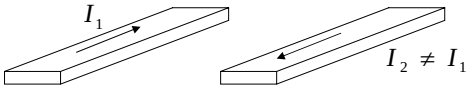
EMI analysis: solution procedure

- **Interconnect impedances depend on complicated return paths.**



- **Unbalanced currents generate most of the interference.**



- **Hence need FULL-BOARD analysis, however simple estimations can be made**

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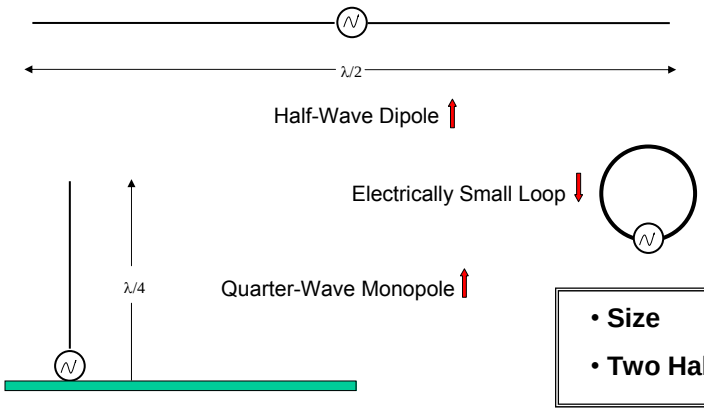
What makes an efficient antenna?



- **Size**
- **Two Halves**

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Estimating Radiated Fields

- **Short dipole** — $E = \mu_0.I.l.f./2r$
  - high impedance
- **Small loop** — $E = \mu_0.I.A.\ \pi.f^2 / 2r.c$
  - low impedance

E = field strength (V/m) , μ_0 = permeability of free space ($4.\pi.10^{-7}$ H/m), I = current (A), l = Length (m), A = area (m^2), f = frequency (Hz), r = distance (m), c = velocity of light (m/s)

Example: **Loop 1cmx1cm, I=100 mA, f=50 MHz, r=10m**

E=30.3 dB(μV/m)

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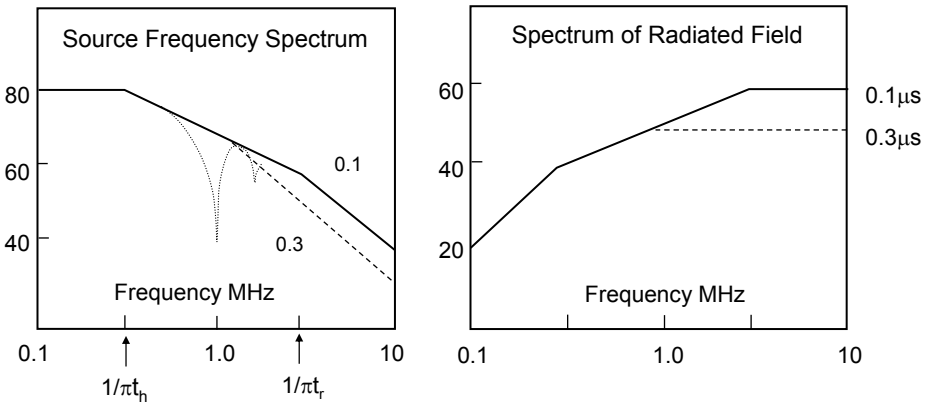
Spectrum of emissions



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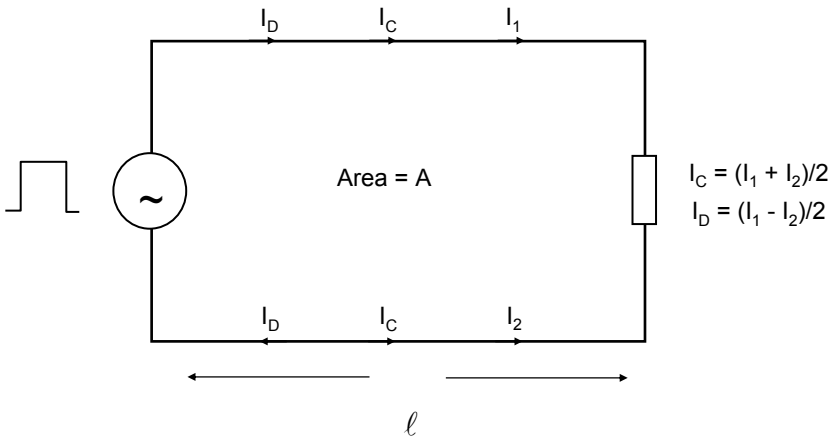
Common & Differential Mode Radiation



- **A smaller common-mode current can produce higher emissions than a larger differential mode current**

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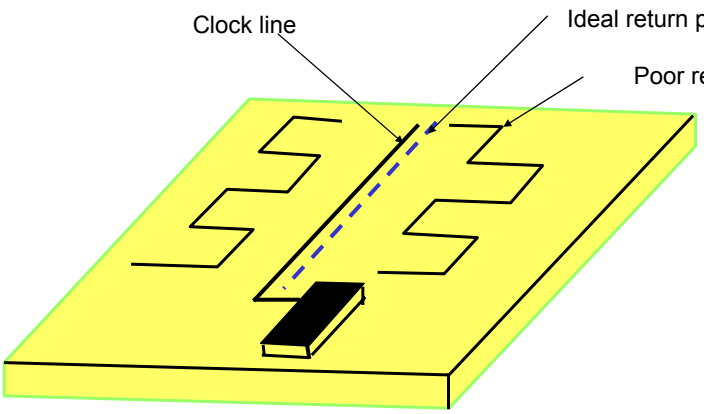
PCB Track Returns



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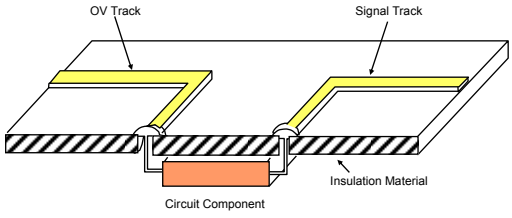
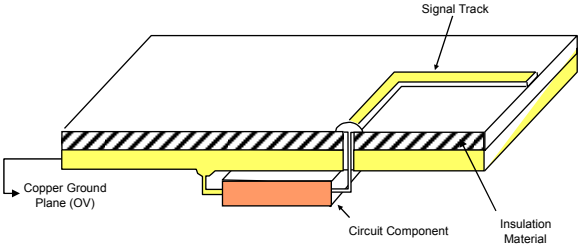
Ground Planes



Double sided Board



Copper Ground Plane Board : 20-30 dB better

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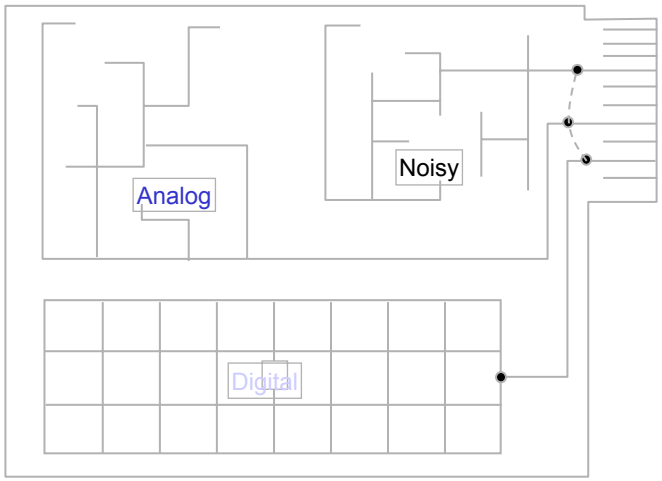
PCB Grounding Scheme



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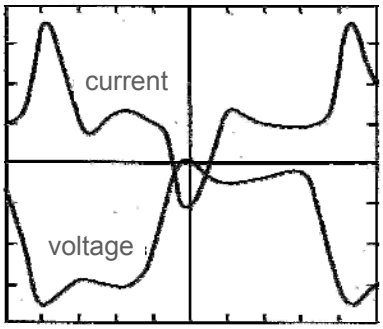
Emission

Loop in circuit
Current level
} → emission

➡ **Current to be derived from voltages**



Remarks

- $I(t) \approx C\frac{dU(t)}{dt}$
  input capacitive
- Current pulses do not vary much with clock frequency

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Agenda

- **Signal and Power Integrity on PCB**
  - Introduction
  - Impedance controlled lines
  - Crosstalk
  - Power integrity issues
  - Decoupling
- **EMI/EMC on PCBs**
- **PCB design guidelines**

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Design Guidelines

- **Most important guidelines**
  - Use controlled impedances when needed with adequate layer stack-up
  - Work with correct circuit models (including parasitics) of lines, passive components and IC-packages in design tools
  - Know where the return currents are flowing and make the current loop well-defined
  - Use balanced lines when possible
  - Keep signal loop areas small
  - Don't locate circuitry between connectors
  - Control transition times in digital signals
  - Never cut gaps in a solid return plane

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Controlling characteristic impedance

- **Stack up defines the PCB layer composition**
- **Stack up defines trace impedance**
- **Keeping power and ground planes together maximizes their capacitive coupling and reduces power supply noise**
- **Extra ground planes can be used to isolate routing layers and reduce crosstalk**
- **Controlled Impedance provides a deterministic method of matching signal termination**
  - It is possible to specify controlled impedance using the appropriate trace width and distance from ground.
  - This also reduces variation in PCB behavior with each hardware build

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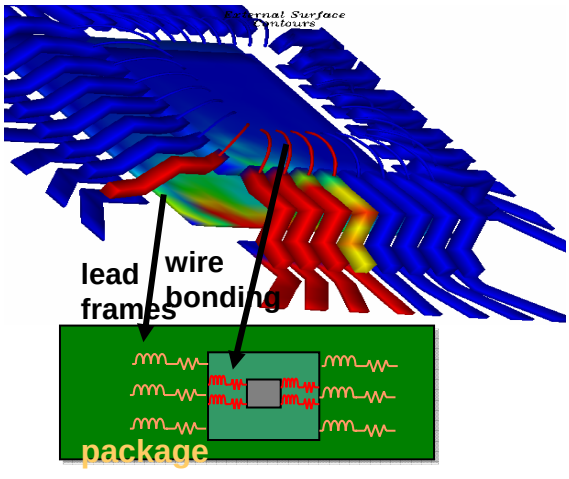
Inductance and Resistance Extraction Example: IC package



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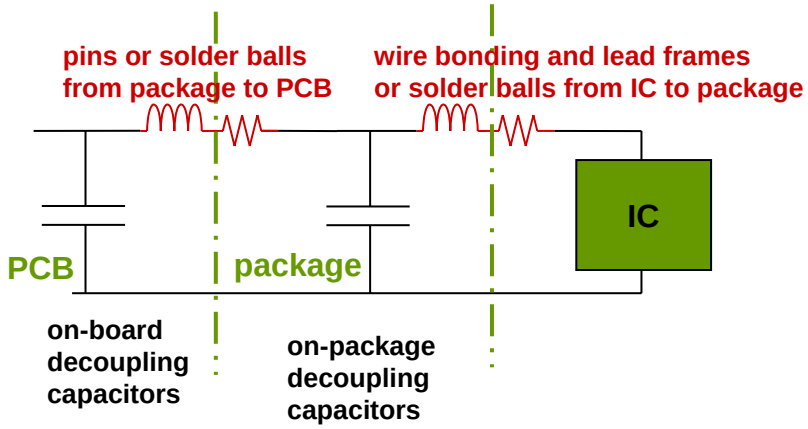
Package circuit model



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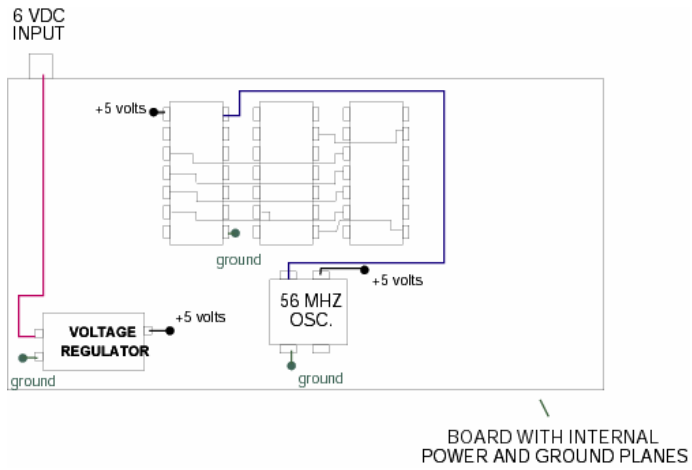
Visualize return currents

Where does the 56 MHz return current flow?



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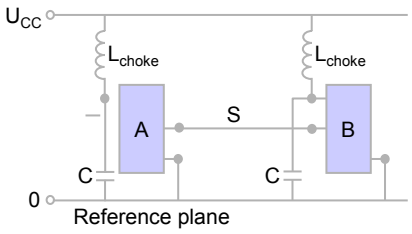
Well-defined current loop

- **Inductances (chokes) prevent current flowing towards U_{cc}**



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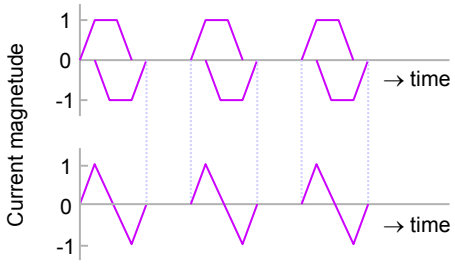
Balanced lines

- **Currents perfectly 180° out of phase and equal in amplitude**
- **Diffcult to realize in very high-speed circuits**
- **Effect of unbalance**



➡ Radiation as large as in unbalanced system

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Keep signal loop areas small

- **Why?**
  - Radiation from circuits
  - Circuit inductance
  - Coupling from circuit

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Keep signal loop areas small

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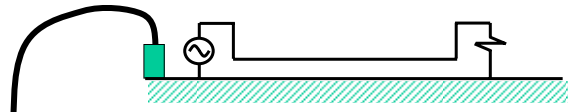
Keep signal loop areas small



CURRENT DRIVEN

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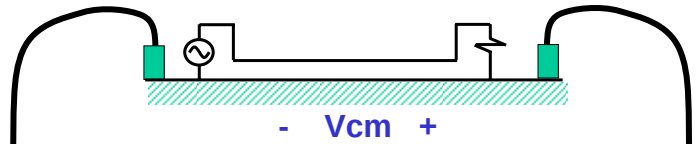
Keep signal loop areas small



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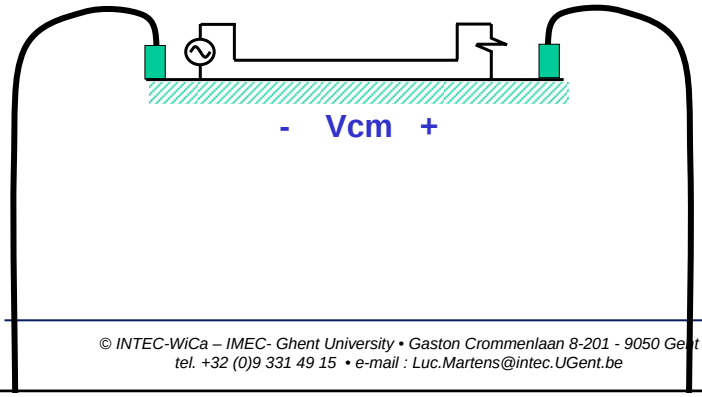
Keep signal loop areas small

Don’t locate HS circuitry between connectors!



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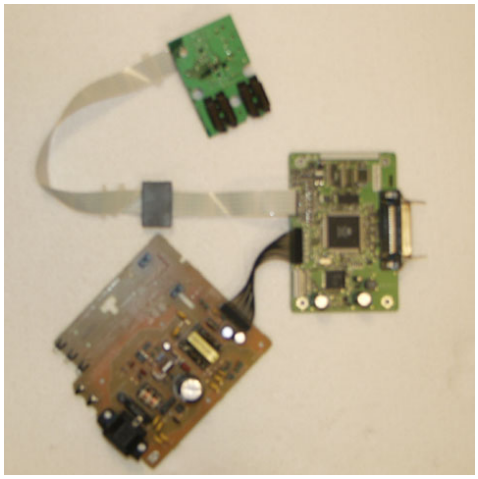

Don’t locate HS circuitry between connectors!

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Chassis ground

- **Provide a good HF chassis ground at connector**
- **Exceptions**
  - When there is no chassis ground
  - When there are no connectors with cables

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(Almost) Never gap a solid ground plane

- **Why?**
  - Creates return path discontinuity
  - Enhances potential differences in ground and crosstalk
  - Makes routing difficult
  - Usually creates more problems than it solves
- **Exeptions**
  - When necessary to prevent common impedance coupling at frequencies below 100 kHz

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Power Plane Design

- **Need to provide low impedance return current path**
- **Provide solid reference planes parallel to the routed signals**
- **Consider return current amplitude when determining power plane thickness**
- **Pair up power and ground layers to provide additional "free" capacitance, reducing power supply noise**
- **Use extra ground planes instead of power planes to isolate sets of routing layers. Use several vias to connect multiple ground layers.**
- **Remember: vias can also create the same effect of a split plane because the reference plane may change**

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Decoupling Considerations

- **Bypassing**
  - Necessary to reduce the effects of ground bounce.
  - Bypass caps provide something like a regulated Power / Gnd at the device package for a short time until the inductance of the plane can be overcome.
  - Transient currents do not have to flow to and from the power supply when the logic device changes states, they flow to and from the caps.
  - Follow IC manufacturer's guideline for appropriate bypass capacitance. Use short wide traces to route capacitor to power / gnd pins on the IC, place capacitor near component
  - Parallel power and ground planes provide another level of bypass capacitance. This power to ground plane capacitance has zero lead inductance and helps reduce power / ground noise at high frequencies. However these planes may resonate.

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Decoupling Considerations (cont.)

- **Bypassing (cont.)**
  - Select capacitors with low resistance and inductance
  - Consider the resonant frequency of the capacitor
  - For high frequency noise, place capacitors near the component being bypassed, ideally next to the power ground pins with dedicated vias for each capacitor

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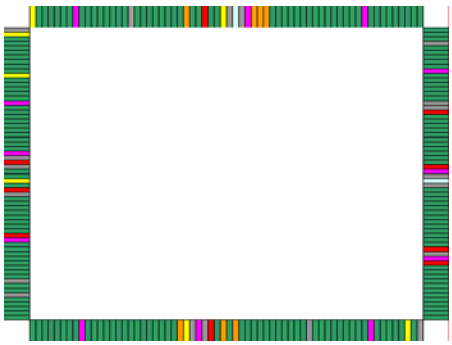
IC Package Effects

- **Example RTSX-S package has poor distribution of power/supply pins around the package**
- **In the diagram shown (CQ256):**
  - **GND: GREY, QTY 19**
  - **Core Supply: Red, QTY 9**
  - **IO Supply: Magenta, QTY 12**
  - **User IO: Green, QTY 201**
- **Inadequate power and ground pins, distributed unevenly around the package. Difficult to define design pin-out without violating switching noise constraints**
- **This effects the IO current return paths and decoupling effectiveness**



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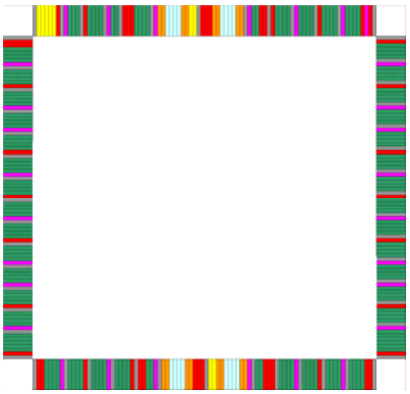
IC Package Effects (cont.)

- RTAXS package has superior distribution of power/supply pins around the package
- In the diagram shown (CQ352):
  - GND: GREY, QTY 56
  - Core Supply: Red, QTY 44
  - IO Supply: Magenta, QTY 29
  - User IO: Green, QTY 179
- Symmetrically distributed power and ground pins around the package, proportional to available IO pins. Far easier to define design pin-out without violating switching noise constraints



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Design of Clock Distribution

- Special care must be taken to ensure proper clock distribution
- Stubs, or excessive loading and route length can cause monotonic glitches
- The use of a clock buffer should be used to provide clean, point to point routing from the clock source to each destination in the clock distribution tree
- Proper termination selection will ensure quiet clock signals
- Other design rules include routing clocks on a “quiet” layer (in between power planes), minimizing the number of layer switches to minimize the effects of via discontinuity
- Matched length clock routing to devices ensures that skew will not decrease timing margins

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Additional design guidelines

- Keep I/O lines short
- Never gap between connectors
- Route highest frequencies on inner layers

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And finally ….

- Design rules won't make you a good circuit board designer
  - Use common sense!
  - Visualize signal current paths
  - Locate antennas and crosstalk paths
  - Be aware of potential EMI sources
  - Seek design advice when you need it

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More information on how to measure on high-frequency PCBs and packages can be found in:

Experimental High-frequency Characterization of Electronic Packaging

Author: Prof. Luc Martens
Publisher: Kluwer Academic Publishers
ISBN number: 0-7923-8307-9

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Venue

Location IMEC vzw
Kapeldreef 75
B-3001 Leuven, BELGIUM
http://www.imec.be/

Date March 27-28, 2006

Abstract

This course will address advanced packaging and assembly technologies. These are strongly driven by the rapid evolution of microelectronics and the increasing complexity of electronic systems. Novel technology trends will be discussed. These have a strong impact on the way electronic systems are designed and manufactured. Electronic packaging is a highly multidisciplinary field, where electrical engineering, mechanical engineering and material science play a key role.

Programme

Programme Chair: Eric Beyne, IMEC vzw

March 27, 2006

13h00-14h00 IC-packaging
Eric Beyne, IMEC vzw

Demands for increased miniaturisation and performance of electronic systems have driven traditional IC packaging technologies to higher levels of sophistication and miniaturisation. In this session, the different styles of IC packages and their evolution will be discussed, from

through-hole to surface mount, from leaded to leadless packages and from 2D to 3D packaging.

14h00-15h00 Wafer Level Packaging
Eric Beyne, IMEC vzw

The ultimate miniaturised package has a size equal to the die size. Such packages may be fabricated at the wafer level, before die singulation. This not only results in the smallest possible packages, but also enables cost reduction. All die on a wafer are simultaneously packaged, in contrast to the sequential tradional package flows. This session will focus on technologies such as flip chip bumping, redistribution and wafer-level CSP. Also possibilities for 3D-WLP technologies will be discussed.

15h15-16h15 Printed circuit board and flexprint technology
Jan Van Fleteren, IMEC vzw/Universiteit Gent

The latest developments in printed circuit board and flexprint technology will be highlighted. For the rigid board technology the focus will be on sequential build-up and microvia technology, and on embedded components (passive and active). New technologies with very thin flexible circuits and stretchable electronic circuits, including embedded components, will be shown, with emphasis on applications in lightweight, wearable electronic systems.

16h15-17h15 Board Level Assembly Technology
Geert Willems, IMEC vzw

The basics of electronic assembly technology will be explained. The session will focus on soldering being the interconnection methodology most widely used in the electronics industry. It will be oriented to lead-free soldering since this will be the soldering technique of the future. The goal of the session is to provide a basic understanding of the different assembly processes used in industrial level electronic assembly and the related boundary conditions, which become significantly more critical in the lead-free era starting July 1st, 2006.

March 28, 2006

09h00-10h30 Reliability issues on package and on board level

Ingrid De Wolf, IMEC vzw

This session starts with an overview of possible packaging-induced IC-failure modes, package failure modes, and interconnect failure modes. This includes both well known failure modes such as 'the pop-corn effect', and less known issues such as 'brittle fracture at low temperatures'. The main failure mechanisms will be explained in more detail. Next several reliability test methods will be described, including testing according to well-known standards, and testing using a failure driven test methodology. Also some techniques that can be used for failure analysis of the packages will be described.

10h30-11h00 Reliability analysis using simulation methods
Bart Vandevelde, IMEC vzw

Simulation methods as virtual prototyping tool will be presented to analyse reliability problems in packaging. Several examples will be shown: wire bonding on Cu/lowK, solder joint interconnection reliability, die and mould cracking during and after processing, mechanical bending of flexible structures, ...

11h15-12h15 Thermal Management
Bart Vandevelde, IMEC vzw and Eric Beyne, IMEC vzw

After introducing the main trends in thermal management for IC packages in electronic systems, the basics of thermal heat transport by conduction, convection and radiation will be briefly explained. The session elaborates on the method of using thermal resistance/impedancesfor packages and systems characterisation, assisted by several practical examples. Also an overview of methods for temperature measuring of IC packages will be given. The session ends with an overview of methods for passive/active cooling of electronic systems.

13h15-14h15 Design-for-Manufacturing: how to make a product out of an electric schematic
Geert Willems, IMEC vzw

An electronic product is a physical entity that must fulfil a multitude of requirements besides performing the functionality that it has been designed for. These

requirements are related to its dimensions, weight, appearance, cost, quality, reliability, reparability, environmental impact, ability to recycle, etc. Based on the electronics assembly session the importance of Design-for-Manufacturing (DFM) as a mandatory practice to achieve high quality, reliable electronic products at low manufacturing costs will be explained. Basic Golden Rules for good DFM practice will be presented. Detailed discussion of design rules lies out of the scope of this session.

14h15-16h30 EMC and signal integrity
Luc Martens, IMEC vzw/Universiteit Gent

As bandwidths of signals increase, parasitics and transmission line effects of boards and packages influence significantly the signal quality. At the same time, the passive interconnections become more vulnerable to external interference. Switching noise and ground bounce effect will also play a role in the signal integrity. The concepts of Electromagnetic Compatability and signal integrity will be explained and illustrated. Rules of thumb for good EMC design will be presented.

Information & registration

For more information and registration, please visit:
http://www.imec.be/tcmwebapp/internet/course.tcm?L=EN_GB&K=MTC&Course=AAAADDP.

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